

### REMARKS

The Examiner is thanked for his indication that claims 1-9 would be allowable if rewritten to overcome the rejections under 35 U.S.C. §112.

Claims 1-9 and 21-24 are presented for consideration. Claims 1 and 21 are independent. Claims 2-9 and 22-24 are dependent. Claims 10-20 have been canceled. Claims 1-7 have been amended. These changes are believed to introduce no new matter, and their entry is respectfully requested. Based on the above Amendment and the following Remarks, Applicants respectfully request that the Examiner reconsider and withdraw all objections and rejections and pass claims 1-9 and 21-24 to allowance.

In paragraph 1 of the Office Action, the Examiner made a Restriction Requirement. Applicants elect Group I for prosecution on the merits. Group I has been defined as claims 1-9. These claims are directed to a fuse sense circuit having an amplifier and a gain stage. Applicants believe that the above election constitutes a full and complete response to the Restriction Requirement and Election of Species. Accordingly, Applicants respectfully request examination on the merits of the elected invention and species.

In paragraph 4, the Examiner objected to claims 1-9 because of formalities. Claims 1-7 have been amended to accommodate this objection. Claims 8-9 properly depend from amended claims. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the objection.

In paragraph 6, the Examiner rejected claims 2-9 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Although Applicants believe claims 2-9 are patentable as written, claims 2-7 have been amended to more particularly point out and distinctly claim the subject matter the Applicants regard as the invention. Claims 8-9 properly depend from patentable claims. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection.

In paragraph 7, the Examiner requested that Figure 1 be designated "Prior Art." A Request for Approval of Drawing Change under 37 C.F.R. §1.121 has been submitted in papers filed herewith accommodating the Examiner's request.

In paragraph 8, the Examiner objected to the drawings, requiring that the word "fuse" and the phrase "enable signal" be added to the drawings. A Request for Approval of Drawing Change under 37 C.F.R. §1.121 has been submitted in papers filed herewith accommodating the Examiner's requirement. Applicants therefore respectfully request that the Examiner reconsider and withdraw the objection.

In paragraph 9, the Examiner rejected claims 21-22 and 24 under 35 U.S.C. 102(b) as being anticipated by Figure 1. Applicants respectfully traverse the rejection. To anticipate, each and every element as set forth in the claim must be found in a single reference.

Claim 21 recites "An apparatus, comprising: an amplifier having an output node; and a gain stage, coupled to the amplifier, having a trip point to track a potential on the output node."

Applicants respectfully submit that Figure 1 fails teach each and every element of claim 21 as the Examiner asserts. For instance, Figure 1 fails to teach a gain stage that has a trip point to track a potential on the output node of an amplifier. Instead, Figure 1 teaches a trip point that fails to track a potential on the output of an amplifier. Applicants submit that therefore that Figure 1 fails to anticipate claim 21. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection.

Claims 22-24 properly depend from a patentable claim (claim 21). As such claims 22-24 are patentable over Figure 1 as well. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection.

In paragraph 10, the Examiner rejected claims 21-24 under 35 U.S. C § 102 (b) as being anticipated by U.S. Patent 5,418, 487 to Armstrong, II ("Armstrong"). Applicants respectfully traverse the rejection.

The Examiner asserts that the P-channel transistor 54 and the N-channel transistor 58 in Armstrong form a gain stage. This is in contrast to Armstrong's clear teaching that the P-channel transistor 54 and the N-channel transistor 58 form an inverter. (Col. 4, lines 42-49). Moreover, the configuration of the P-channel transistor 54 and the N-channel transistor 58 as the inverter does not have a trip point that tracks the output 32 of the amplifier. Applicants submit that therefore that Armstrong fails to anticipate claim 21. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection.

Claims 22-24 properly depend from a patentable claim (claim 21). As such claims 22-24 are patentable over Armstrong as well. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection.

**CONCLUSION**

Applicant submits that all grounds for objection and rejection have been properly traversed or accommodated. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw all presently outstanding objections and rejections and pass claims 1-9 and 21-24 to allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: December 14, 2001

Jan Carol Little  
Jan Carol Little  
Reg. No.: 41,181

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, CA 90025-1026  
(206) 292-8600

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Sharon E. Farnus

Name of Person Mailing Correspondence

Sharon Farnus 12/14/01  
Signature Date

### VERSION OF CLAIMS WITH MARKINGS

1. (Amended) An apparatus, comprising:  
first circuit branch;  
second circuit branch, coupled to the first circuit branch in a current mirror configuration;  
an amplifier, coupled to the second circuit branch, comprising a scaled replica of the first branch and an amplifier output node; and  
an enable node coupled to the first circuit branch, the second circuit branch, and the [post] amplifier to indicate a first logical state at the amplifier output node if the first circuit branch is programmed and the second circuit branch is un-programmed and to indicate a second logical state at the amplifier output node if the first circuit branch is un-programmed and the second branch is programmed.
2. (Amended) The apparatus of claim 1, [further comprising] wherein the first, second, and third circuit branches include:  
first, second, and third resistances, respectively, each having one terminal coupled to a first voltage;  
first, second, and third current mirror devices, respectively, each having one terminal coupled to an opposite terminal of the first, second, and third resistances, respectively, the third current mirror device matching the first current mirror device, the first current mirror device coupled to the second current mirror device in a current mirror configuration; and  
first, second, and third loads, respectively, each having one terminal coupled to an opposite terminal of the first, second, and third current mirror devices, respectively, a second terminal coupled to a second voltage, the third load matching the first load, and a third terminal coupled to the enable node.
3. (Amended) The apparatus of claim 2, further comprising a second branch output node coupled to the second branch and the first branch current mirror, a second branch output node potential to decrease if the second resistance increases relative to the first resistance and to increase if the second resistance decreases relative to the first resistance, [an] the amplifier output node potential being equivalent to the second branch output node potential if the second resistance is equivalent to the first resistance.

4. (Amended) The apparatus of claim 2, wherein the amplifier is to trip at a predetermined trip point associated with an amplifier input voltage, the [further comprising a] trip point to sufficiently track a potential on the first current mirror device terminal coupled to the first resistance.

5. (Amended) The apparatus of claim 2, wherein the amplifier is to trip at a predetermined trip point associated with an amplifier input voltage, the [further comprising a] trip point to sufficiently track a potential on the first current mirror device terminal coupled to the first resistance and to trip the amplifier if the first resistance is approximately equal to the second resistance.

6. (Amended) The apparatus of claim 2, wherein the amplifier is to trip at a predetermined trip point associated with an amplifier input voltage, the [further comprising a] trip point to sufficiently track a potential on the first current mirror device terminal coupled to the first resistance and to trip the amplifier if the potential on the first current mirror device terminal coupled to the first resistance is approximately equal to the second branch output node potential.

7. (Amended) The apparatus of claim [2, further comprising the] 3, wherein an amplifier output node potential is [to be] equivalent to the second branch output node potential if the first resistance is approximately equal to the second resistance.

8. The apparatus of claim 2, the first, second, and third resistances each further comprising a fuse element.

9. The apparatus of claim 1, the first, second, and third current mirror devices each further comprising p-channel material.

10. (Canceled) A resistance sense circuit, comprising:  
first circuit branch;  
second circuit branch coupled to the first branch in a current mirror configuration;  
an amplifier coupled to the second circuit branch, the amplifier comprising a load having its gate coupled to a first voltage and its source coupled to a second voltage, and an output node; and  
an enable node coupled to the first circuit branch and the second circuit branch to turn the current mirror on to enable the resistance sense circuit to indicate a logical state at the output node if an enable signal is asserted on the enable node, the first circuit branch is unprogrammed and the second circuit branch is programmed.
11. (Canceled) The resistance sense circuit of claim 10, the output node further to indicate a value approximately equal to the first voltage if the enable signal is asserted and to indicate a value approximately equal to the second voltage if the enable signal is de-asserted.
12. (Canceled) The resistance sense circuit of claim 10, the first resistance further comprising a resistor and the second resistance further comprising a fuse element.
13. (Canceled) The resistance sense circuit of claim 10, further comprising:  
first input node coupled to the second circuit branch to program the second circuit branch with a first logical state; and  
second input node coupled to the first circuit branch to program the first circuit branch with a second logical state.

14. (Canceled) The resistance sense circuit of claim 10, further comprising:  
first resistance and second resistance each having one terminal coupled to a voltage;  
first and second current mirror device each having one terminal coupled to an  
opposite terminal of the first and second resistance, respectively, the first current mirror  
device coupled to the second current mirror device in a current mirror configuration;  
third current mirror device matching the first current mirror device, the third current  
mirror device having a gate coupled to a second circuit branch output node and a source  
coupled to the voltage; and  
first and second load each having one terminal coupled to an opposite terminal of the  
first and second current mirror device, respectively.
15. (Canceled) The resistance sense circuit of claim 14, further comprising:  
first input node coupled between the second current mirror device and the second  
resistance to program the second resistance with a first logical state; and  
second input node coupled between the first current mirror device and the first  
resistance to program the first resistance with a second logical state.
16. (Canceled) An apparatus, comprising:  
a sense amplifier;  
a current mirror having a current mirror output node and a current mirror drain; and  
a differential amplifier coupled to the sense amplifier via the current mirror output  
node, the differential amplifier to change states if a potential on the current mirror output  
node is approximately equal to a potential on the current mirror drain.
17. (Canceled) The apparatus of claim 16, further comprising first resistance and second  
resistance coupled to a current mirror source.
18. (Canceled) The apparatus of claim 16, further comprising first resistance and second  
resistance coupled to a current mirror source, the first and second resistances comprising p-  
channel material.

19. (Canceled) The apparatus of claim 16, further comprising:  
first resistance coupled to a current mirror source;  
second resistance coupled to the current mirror source; and  
an enable node coupled to the current mirror drain to enable the differential amplifier to indicate a logical state at a differential amplifier output node if an enable signal is asserted on the enable node, the first circuit resistance is un-programmed and the second resistance is programmed.
20. (Canceled) The apparatus of claim 16, the differential amplifier further comprising a second current mirror output node coupled to an inverting input of the differential amplifier.
21. An apparatus, comprising:  
an amplifier having an output node; and  
a gain stage, coupled to the amplifier, having a trip point to track a potential on the output node.
22. The apparatus of claim 21, the amplifier comprising a sense branch coupled to a reference branch in a current mirror configuration.
23. The apparatus of claim 22, the gain stage comprising a scaled replica of the reference branch or the sense branch.
24. The apparatus of claim 22, further comprising first and second voltages each coupled to the amplifier and the gain stage.

### **VERSION OF SPECIFICATION WITH MARKINGS**

Figure 4 shows an exemplar fuse sense circuit 400 with a matched gain stage. The fuse sense circuit 400 has a post amplifier device 426 with its source tied to the voltage and a post amplifier load 422 with its gate tied to the voltage [332] 232 instead of a sense enable signal input node [260] 560. This embodiment allows the post amplifier load 422 to pull down a post amplifier output node 450 when the sense amplifier 402 is powered down (*i.e.*, when the sense enable signal is de-asserted).